

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	762	(712/23).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/05 13:22
S2	486	(712/215).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/05 13:22
S3	0	(superscalar\$1) same (issu\$3 with way\$1 with group\$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/05 13:23
S4	7	(issu\$3 with way\$1 with (instruction\$1 near4 group\$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/05 13:26
S5	0	(issu\$3 with (instruction\$1 near4 group\$3)) same (mutiple\$1 near4 (process\$3 or function\$3) near4 (unit\$1 or device\$1 or element\$1))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/05 13:27
S6	0	(issu\$3 with instruction\$1 with (simultaneous\$2 or concurrent\$2)) same (mutiple\$1 near4 (process\$3 or function\$3) near4 (unit\$1 or device\$1 or element\$1))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/05 13:27
S7	0	(issu\$3 with instruction\$1 with (simultaneous\$2 or concurrent\$2)) same (mutiple\$1 near4 (process\$3 or function\$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/05 13:28
S8	0	(issu\$3 with instruction\$1 with (simultaneous\$2 or concurrent\$2)) same (mutiple\$1 with (process\$3 or function\$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/05 13:28
S9	1	(issu\$3 with instruction\$1 with (simultaneous\$2 or concurrent\$2)) and (mutiple\$1 with (process\$3 or function\$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/05 13:28
S10	132	(issu\$3 with instruction\$1 with (simultaneous\$2 or concurrent\$2)) and (integer near4 (float\$3?point\$1))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/05 13:29
S11	16	(issu\$3 with instruction\$1 with (simultaneous\$2 or concurrent\$2)) same (integer near4 (float\$3?point\$1))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/05 13:29

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S12	8	(("6038656") or ("5752070") or ("6044061") or ("5832303") or ("6230228") or ("5802055") or ("6279065") or ("6301630")).PN.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/05 13:32
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chip + CMOS + GaAs + SiGe

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[Preferences](#)**Web**Results 1 - 10 of about 92,100 for chip + CMOS + GaAs + SiGe. (0.43 seconds)**SiGe and CMOS target GaAs dominance of cellular PA slots (May 2004 ...**Although **GaAs** continues to dominate in cellular PAs, several suppliers hope that their new products designed in **SiGe** and **CMOS** may soon start to appear in ...

www.compoundsemiconductor.net/articles/magazine/10/5/3/1 - 24k -

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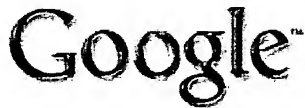
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On-chip **CMOS** decode logic facilitates both 1.8 V and 2.75 V ... significant performance advantages over competing processes such as **GaAs**, **SiGe** BiCMOS ...www.peregrine-semi.com/articles/2005/2005_pr_10-3.pdf - [Similar pages](#)**[PDF] Will GaAs Survive for Wireless PA's ??**File Format: PDF/Adobe Acrobat - [View as HTML](#)Keywords: **SiGe**, **CMOS**, **GaAs**, GaN, WLAN. Abstract. **SiGe** HBT's and Si **CMOS** continue to capture more ... this range (0.7 W/mm) four **GaAs** chips achieved 250 W of ...www.gaasmantech.org/Digests/2005/2005papers/1.3.pdf - [Similar pages](#)**Mayo SPPDG Home Page**... in the GaInAs base and collector regions is higher than in Si, **SiGe**, or **GaAs**. ...**CMOS** and Silicon Germanium Bipolar HBT Technologies in Combination ...

www.mayo.edu/sppdg/emerging_device_ic_technologies.html - 21k -

[Cached](#) - [Similar pages](#)**[PDF] LOOKING BEYOND MONOLITHIC**File Format: PDF/Adobe Acrobat - [View as HTML](#)bipolar performance, eclipsing **CMOS**. **SiGe** BiCMOS is. giving product designers the performance of **GaAs**. with integration levels and cost-effectiveness close ...www.jazzsemi.com/news_events/whitepapers/AWR_SiP.pdf - [Similar pages](#)**SiGe Introduction**The real strength of **SiGe** lies in its ability to integrate analog, RF and digital on a single chip using existing **CMOS** fabs. This is not possible with any ...www.eng.auburn.edu/~guofu/sige_intro.htm - 15k - [Cached](#) - [Similar pages](#)

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simulation + netlist + HDL

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[Preferences](#)**Web**Results 1 - 10 of about 118,000 for simulation + netlist + HDL. (0.46 seconds)**Simulation Points**

A testbench is **HDL** code written for the **simulator** that will instantiate the design **netlist(s)**, initialize the design and then apply stimuli to verify the ...
toolbox.xilinx.com/docsan/xilinx4/data/docs/sim/simu4.html - 20k -
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Setting HDL and Simulation Options [Platform Studio]

The **HDL** setting is used to specify your preferred **HDL** language. XPS generates your synthesis and **simulation netlist** in this **HDL** language. ...

toolbox.xilinx.com/docsan/xilinx8/EDKHelp/platform_studio/html/ps_p_prf_setting_hdl_simulation_options.htm - 7k -
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Synopsys Simulations - Mixed-HDL Simulation White Paper

To meet the mixed-**HDL simulation** needs of the design community, Synopsys has ...
 With Scirocco-MX, VHDL designers only have to generate a Verilog **netlist** of ...
www.synopsys.com/products/simulation/mixed_hdl_wp.html - 19k -
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Aldec Inc. - The Design Verification Company - Products - Active ...

... library and **netlist** automatically attached to Active-**HDL** project ... Simulink®
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www.aldec.com/products/active-hdl/multimediamdemo/ - 42k - [Cached](#) - [Similar pages](#)

Aldec Inc. - The Design Verification Company - Products - Active ...

Active-**HDL's** has a rich set of debugging and **simulation** results ... design in
 Active-**HDL** is enabled by support of the EDIF **netlist** format and legacy design ...
www.aldec.com/products/active-hdl/ - 34k - [Cached](#) - [Similar pages](#)

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DeepChip Homepage

Yes we use mixed-**HDL**, mainly because other groups in the company use Verilog, ...
 We use mixed **simulation** for ASIC **netlist simulation** (if emulation is not ...
www.deepchip.com/items/dvcon05-02.html - 21k - [Cached](#) - [Similar pages](#)

Winbond-Empowering Partners-Winning Products-Foundry Service

Pre-layout **Simulation** starts after the **netlist** passes criteria of the design-rule checker. **Netlist** Conversion. For design in **HDL**, Winbond provides Synopsys ...
www.winbond.com/e-winbondhtm/partner/b_2_i_1.htm - 36k - [Cached](#) - [Similar pages](#)

[PDF] Simulate the Gate-Level HDL Netlist

File Format: PDF/Adobe Acrobat - [View as HTML](#)

Since the **HDL netlist** of the synthesized circuit consists of target library gates, you need to specify the library as. directory where the **simulation** models ...



chip + CMOS + GaAs + SiGe

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SiGe HBT technology: a new contender for Si-based RF and microwave circuit applications - group of 4 »

JD Cressler - IEEE Transactions on Microwave Theory and Techniques, 1998 - [ieeexplore.ieee.org](#)
 ... of **SiGe** HBT's with advanced Si **CMOS** to form ... to 64-Mb dynamic random-access memory (DRAM) **chips**. ... InP fill important niche markets today (eg, **GaAs** MESFET's ...
 Cited by 112 - [Web Search](#) - [BL Direct](#)

1.8 Million Transistor CMOS ASIC Fabricated in a SiGe BiCMOS Technology - group of 3 »

RA Johnson, MJ Zierak, KB Outama, TC Bahn, AJ ... - IEDM Tech. Dig, 1998 - [ieeexplore.ieee.org](#)
 ... of integration and evolve toward a single **chip** solution. ... technologies for one system such as **GaAs** for the ... rf components, while using VLSI silicon **CMOS** for the ...
 Cited by 16 - [Web Search](#)

Integrated Circuit Technology Options for RFIC's-Present Status and Future Directions - group of 5 »

LE Larson... - 1998 - [ieeexplore.ieee.org](#)
 ... and bipolar junction transistors (BJT's), Si/**SiGe** HBT's and **GaAs** MESFET's ... path, resulting in a highly integrated "single-**chip CMOS** radio" sometime ...
 Cited by 98 - [Web Search](#) - [BL Direct](#)

A fully-monolithic SiGe differential voltage-controlled oscillator for 5 GHz wireless applications - group of 2 »

JO Plouchart, H Ainspan, M Soyuer, A Ruehli - Proceedings of IEEE 2000 RFIC Symposium, 2000 - [ieeexplore.ieee.org](#)
 ... Fig 5 shows the microphotograph of the **chip**. ... monolithic VCO's in different technologies including **GaAs** MESFET [13 ... 3], silicon bipolar [2], 0.35-um **CMOS** [4], [6 ...
 Cited by 16 - [Web Search](#)

m CMOS 10-Gb/s Multiplexer/Demultiplexer ICs Using Current Mode Logic with Tolerance to Threshold ... - group of 6 »

A Tanabe, M Umetani, I Fujiwara, T Ogura, K ... - IEEE JOURNAL OF SOLID-STATE CIRCUITS, 2001 - [ieeexplore.ieee.org](#)
 ... 10-GHz 8 B-mul- tiplexer/demultiplexer **chip** set for ... 1 multiplexer/1:8 demultiplexer," in IEEE **GaAs** IC Symp ... s demultiplexer IC in 0.18- m **CMOS** using current ...
 Cited by 30 - [Web Search](#) - [BL Direct](#)

Foundation of rf CMOS and SiGe BiCMOS technologies - group of 6 »

JS Dunn, DC Ahlgren, DD Coolbaugh, NB Feilchenfeld ... - IBM JOURNAL OF RESEARCH AND DEVELOPMENT, 2003 - [research.ibm.com](#)
 ... Wireless LAN **chip** set, Three **SiGe** **chips** and one **CMOS** **chip** to replace eight **GaAs** **chips**, Commercial production part in PCM-CIA cards, [11], Intersil. ...
 Cited by 10 - [Cached](#) - [Web Search](#) - [BL Direct](#)

A 2. 4-GHz-band 1. 8-V operation single-chip Si-CMOS T/R-MMIC front-end with a low insertion loss ... - group of 4 »

K Yamamoto, T Heima, A Furukawa, M Ono, Y ... - IEEE Journal of Solid-State Circuits, 2001 -



simulation + netlist + HDL

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ScholarResults 1 - 10 of about 2,330 for **simulation + netlist + HDL**. (0.09 seconds)JHDL-An **HDL** for Reconfigurable Systems - group of 9 »

P Bellows, B Hutchings - IEEE Symposium on Field-Programmable Custom Computing ..., 1998 - doi.ieeecomputersociety.org

... sen to name this system, JHDL, for Just another **HDL**. ... Partial Reconfiguration: Software **Simulation** ... This constraint helps the PRSocket develop a **netlist**, and is ...

Cited by 117 - [Web Search](#)

A Formal **HDL** and its Use in the FM9001 Verification - group of 3 »

WA Hunt, BC Brock - Philosophical Transactions: Physical Sciences and ..., 1992 - JSTOR

... The **simulator**, when given a **netlist**, a module reference ... clock **simulator** provides a circuit **simulation** capability. **HDL** circuits are written using the Lisp quote ...

Cited by 46 - [Web Search](#) - [Library Search](#)

EXPRESSION: A Language for Architecture Exploration through Compiler/Simulator Retargetability - group of 14 »

A Halambi, P Grun, V Ganesh, A Khare, ND Dutt, A ... - DATE, 1999 - ieeexplore.ieee.org

... wherein the net-list of the target processor is described in a **HDL** like language. ...

Using this information, both the **netlist** for **simulator** and reservation ...

Cited by 182 - [Web Search](#)

A Reconfigurable Logic Machine for Fast Event-Driven **Simulation** - group of 11 »

J Bauer, M Bershteyn, I Kaplan, P Vyedn - PROC DES AUTOM CONF. pp. 668-671. 1998, 1998 - doi.ieeecomputersociety.org

... a compiler that can compile a behavioral Verilog **HDL** description of ... real time operating system to manage behavioral **simulation** and logic **netlist** emulation. ...

Cited by 20 - [Web Search](#) - [BL Direct](#)

Defect-Oriented Mixed-Level Fault **Simulation** of Digital Systems-on-a-Chip Using **HDL**. - group of 11 »

MB Santos, JP Teixeira - DATE, 1999 - doi.ieeecomputersociety.org

... DO fault **simulation** for SOCs, using **HDL**, was presented. ... T. Larrabee, "Charge-Based Fault **Simulation** for CMOS ... F. Brglez, H. Fujiwara, "A Neutral **Netlist** of 10 ...

Cited by 10 - [Web Search](#)

A Transaction Based Unified **Simulation**/Emulation Architecture for Functional Verification - group of 11 »

C Selvidge, M Kudlugi, S Hassoun, D Pryor - Proceedings of the 38th Design Automation Conference, 2001 - ieeexplore.ieee.org

... event-driven behavioral **simulation**[2]. When synchro- nizing aC **simulation** with an **HDL simulator** modeling a detailed **netlist**, the latter becomes the bottleneck. ...

Cited by 9 - [Web Search](#)

Pre- and postsynthesis **simulation** mismatches - group of 6 »

H Howe - The 1997 6 th International Verilog **HDL** Conference, IVC'97, 1997 - doi.ieeeecs.org

... level **netlist**, and discusses some possible sources of **simulation** mismatches due to RTL model ambiguities. This document assumes you understand **HDL** modeling ...